GAP\_CMP

Revision History

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| --- | --- | --- | --- |
| Revision Number | Date | Description of Change | Author |
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Table of Contents

[GAP\_CMP 2](#_Toc116648545)

[Introduction 2](#_Toc116648546)

[Main features 2](#_Toc116648547)

[Functional Details 2](#_Toc116648548)

[Block Diagram 2](#_Toc116648549)

[Compare flow 4](#_Toc116648550)

# GAP\_CMP

## Introduction

GAP\_CMP is designed for functional safety goal, in order to monitor whether ADC works normally, the system use an auxiliary ADC converts along with the main ADC, GAP\_CMP automatically compares the gap of the two ADC measurement results with configurable threshold, if the gap exceeds the given range, a warning will be asserted.

### Main features

The GAP\_CMP module has the following features:

• Configurable gap threshold of CELL’s measurement

• Configurable gap threshold of others(GPIO’s) measurement

• Configurable gap filter range of CELL’s measurement

## Functional Details

### Block Diagram



Fig GAP\_CMP block diagram

GAP\_CMP I/O signals description shows in table.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pin Name | Direction | Width | Default Value | Description |
| **resetb\_SR\_CLK\_SLOW** | Input | 1b' | 1'b1 | Asynchronous power on reset |
| **CLK\_SLOW\_SC** | Input | 1b' | 1'b0 | 256K |
| **SGLE\_ADC\_GO\_DLY** | Input | 1b' | 1'b0 | ADC\_SGLE\_GO delay |
| **CNTI\_ADC\_GO\_DLY** | Input | 1b' | 1'b0 |  |
| **MON\_WAKE\_GO** | Input | 1b' | 1'b0 | ADC single conversion go |
| **RR\_END** | Input | 1b' | 1'b0 | GAP\_CMP shall compare the gap between AUX\_ADC\_DATA\_LPF and ADC\_DATA\_LPF with CELL\_GAP\_THRESH when RR\_END is high |
| **D2A\_CELL\_ADC\_EN** | Input | 1b' | 1'b0 | ADC enable |
| **CELL\_GAP\_THRESH\_REG** | Input | 5b' | 5'h0 | CELL\_GAP\_THRESH shall cover from 20mV to 180mV, 5mV step |
| **OTH\_GAP\_THRESH\_REG** | Input | 3b' | 3'h0 | OTH\_GAP\_THRESH shall cover from 1% to 8%, 1% step |
| **CELL\_GAP\_DEGL\_REG** | Input | 5b' | 5'h0 | CELL\_GAP\_DEGL shall cover from 1 to 32 |
| **ADC\_DATA\_LPF\_CH1  -ADC\_DATA\_LPF\_CH18** | Input | 16b' | 16'h8000 | Main ADC converted data of CELL1-CELL18 with DLPF |
| **ADC\_DATA\_GPIO1  -ADC\_DATA\_GPIO12** | Input | 16b' | 16'h8000 | Main ADC converted data of GPIO1-GPIO12 |
| **AUX\_ADC\_DATA\_LPF\_CH1  -AUX\_ADC\_DATA\_LPF\_CH18** | Input | 16b' | 16'h8000 | Auxiliary ADC converted data of CELL1-CELL18 with DLPF |
| **AUX\_ADC\_DATA\_GPIO1  -AUX\_ADC\_DATA\_GPIO12** | Input | 16b' | 16'h8000 | Auxiliary ADC converted data of GPIO1-GPIO12 |
| **CELL\_GAP\_FLT** | Output | 18b' | 18'h0 | Over gap threshold flag of CELL1-CELL18 |
| **OTH\_GAP\_FLT** | Output | 12b' | 12'h0 | Over gap threshold flag of other channel |

### Compare flow

GAP\_CMP reloads the values of CELL\_GAP\_THRESH\_REG, OTH\_GAP\_THRESH\_REG and CELL\_GAP\_DEGL\_REG into CELL\_GAP\_THRESH, OTH\_GAP\_THRESH and CELL\_GAP\_DEGL when ADC\_GO\_DLY(includes ADC\_SGLE\_GO\_DLY and ADC\_CNTI\_GO\_DLY) or MON\_WAKE\_GO is detected high.**TSR001[GAP\_CMP]**

GAP\_CMP calculates the gap between AUX\_ADC\_DATA\_LPF and ADC\_DATA\_LPF firstly, compares each gap of CELL18-CELL1 with CELL\_GAP\_THRESH when RR\_END is detected high. If any gap takes place over range, the filter counter of corresponding CELL will increased by 1, while the gap is not over range, the filter counter will decreased by 1, until the counter reaches CELL\_GAP\_DEGL, a corresponding warning flag will be asserted to CELL\_GAP\_FLT register. CELL\_GAP\_THRESH covers range from 20mV to 180mV by 5mV per step, the LSB for Cn-Cn-1 is typical 200uV and CELL\_GAP\_DEGL covers from 1 to 32. **TSR001[GAP\_CMP]**

After the completion of all CELLs gap comparison, GAP\_CMP continues to compare the gap between AUX\_OTH\_ADC\_DATA and OTH\_ADC\_DATA with OTH\_GAP\_THRESH. Any gap of GPIO channels over range, the corresponding warning flag will be output to OTH\_GAP\_FLT. OTH\_GAP\_THRESH covers range from 1% to 8%, by 1% step, the LSB for GPIO voltage ratio measurement shall be 100uV /2.5V(40uV). **TSR001[GAP\_CMP]**

GAP\_CMP compare flow is shown in Fig2.

As shown in Fig2, MON\_ADC\_GO and ADC\_GO\_DLY need to be synchronized and captured the rising edge to refresh GAP THRESHOLD registers by CLK\_SLOW\_SC(256K). If MON\_ADC\_GO or ADC\_GO\_DLY comes during the compare process(comparison enable[cmp\_en] is high), GAP THRESHOLD registers can not be refreshed immediately until the compare process is finished(cmp\_en is low). After ADC conversion is done, and the synchronization signal of RR\_END is detected high, cmp\_en will be set to high to enable the 5bits counter automatically increment 1 by CLK\_SLOW\_SC. When the counter is less than 19, GAP\_CMP starts to calculate the gaps of main ADC and auxiliary ADC CELL’s measurement results and compare the gaps with CELL threshold. Otherwise GAP\_CMP calculates the gaps of main ADC and auxiliary ADC GPIO’s measurement results and compare the gaps with GPIO threshold. When the counter reaches 31, the counter is cleared to 0 and cmp\_en is set to 0.



Fig C\_OW\_CTRL state machine flow

Notes that although ADC\_CNTO\_GO\_DLY only initiates continuous conversion of CELLs, GPIO channels are not converted and no new measurements are available. GAP\_CMP still need to calculate the gap and compare the gap with threshold by previous converted results.